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Patent
Attorney's Docket No. 0023-0020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Ross HEITKAMP et al.	)	Group Art Unit: 2111
	)	
Application No.: 09/751,449	)	Examiner: T. Cleary
	)	
Filed: January 2, 2001	)	
	)	
For: MULTI-MASTER AND DIVERSE SERIAL BUS IN A COMPLEX ELECTRICAL SYSTEM	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
220 20th Street S.
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Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Transmitted herewith in triplicate is an Appeal Brief in support of the Notice of Appeal filed June 14, 2004.

Enclosed is a check for ☐ $165.00 ☒ $330.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070. This paper is submitted in triplicate.

Respectfully submitted,

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Date: August 13, 2004

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

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Arlington, VA 22202

Sir:

This Appeal Brief is submitted in response to the final rejection, mailed March 26, 2004, and in support of the Notice of Appeal, filed June 14, 2004.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Juniper Networks, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-22, 24, and 25 are pending in this application. Claims 20 and 21 are objected to as being dependent on a rejected claim but otherwise are indicated as containing allowable subject matter. Claims 1-19, 22, 24, and 25 were finally rejected in the Final Office Action of March 26, 2004 and are the subject of this appeal. A copy of the pending claims is attached in the Appendix.

IV. STATUS OF AMENDMENTS

No amendments were filed after the Final Office Action of March 26, 2004.

V. SUMMARY OF THE INVENTION

As discussed in the "Background of the Invention" section of the application, serial busses, such as two-wire serial busses, may be used to exchange information between different electrical components. (Spec., pages 2-3; Figs. 1A and 1B). As discussed in the specification, however, these conventional implementations can be problematic when a large number of devices are connected to the bus or when attempting to connect devices on different circuit boards.

The present invention, as recited in the various claims, provides systems and devices for implementing a bus over multiple circuit boards. Claim 1, for example, is directed to a system that includes a master control processor and a bus controller connected to the master control processor. (Spec., Fig. 4, elements 407 and 410; page 8, lines 12-21). The master control processor and

the bus controller are on a first circuit board. The bus controller implements a serial bus interface between the master control processor and a plurality of serial bus devices, such as a voltage monitor 510 or temperature sensor 511 (Spec., Fig. 5). The serial bus devices may be additional circuit boards connected to the serial bus interface through a midplane. (Spec., pages 8-9, midplane 310 (Fig. 3), additional circuit boards 402-405 (Fig. 4)). Each of the additional circuit boards may include a switch that connects the circuit board to the first circuit board through the serial bus interface when the switch is in a first state and electrically isolates the circuit board from the first circuit board when the switch is in a second state. (Spec., page 10, lines 9-11, switch 430 (Fig. 4)). Each of the additional circuit boards additionally includes local control logic for outputting a signal for controlling the state of the switch. The local control logic controls the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state. (Spec., page 10, lines 4-11; local control logic 432 (Fig. 4)).

VI. ISSUES

A. Whether claims 1 and 2 are unpatentable under 35 U.S.C. § 103(a) in view of U.S. Patent No. 6,526,464 to Jobs et al. ("Jobs"), U.S. Patent No. 6,381,239 to Atkinson et al. ("Atkinson"), and U.S. Patent No. 5,957,985 to Wong et al. ("Wong").

B. Whether claims 3 and 6 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, and Wong, and additionally in view of U.S. Patent No. 6,301,623 to Simpson et al. ("Simpson").

C. Whether claims 4 and 5 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, Wong, and Simpson and further in view of U.S. Patent No. 6,532,500 to Li et al. ("Li") and U.S. Patent No. 6,122,756 to Baxter et al. ("Baxter").

D. Whether claims 7 and 8 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, and Wong, and further in view of U.S. Patent No. 4,845,736 to Posner et al. ("Posner").

E. Whether claims 9, 10, and 13 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, and U.S. Patent No. 6,330,614 to Aggarwal et al. ("Aggarwal").

F. Whether claims 11 and 12 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, Aggarwal, and further in view of Wong.

G. Whether claims 14 and 17 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, Aggarwal, and Simpson. Whether claims 15 and 16 are unpatentable under 35 U.S.C. § 103(a) in view of Jobs, Atkinson, Aggarwal, and Simpson, and further in view of Li and Baxter.

H. Whether claim 18 is unpatentable under 35 U.S.C. § 103(a) in view of Atkinson, Posner, and Wong.

I. Whether claim 19 is unpatentable under 35 U.S.C. § 103(a) in view of Atkinson, Posner, and Wong.

J. Whether claim 22 is unpatentable under 35 U.S.C. § 103(a) in view of Atkinson, Posner, and Wong, and further in view of U.S. Patent No. 5,185,693 to Loftis et al. ("Loftis").

K. Whether claim 24 is unpatentable under 35 U.S.C. § 103(a) in view of Atkinson, Posner, and Wong, and further in view of Li.

L. Whether claim 25 is unpatentable under 35 U.S.C. § 103(a) in view of Atkinson, Posner, and Wong, and further in view of Baxter.

VII. GROUPING OF CLAIMS

Appellants are satisfied to let claims 1 and 2 stand or fall together. Claims 3 and 5 stand or fall together as a separate group. Claims 4 and 5 stand or fall together as a separate group. Claims 7 and 8 stand or fall together as a separate group. Claims 9, 10, and 13 stand or fall together as a separate group. Claims 11 and 12 stand or fall together as a separate group. Claims 14-17 stand or fall together as a separate group. Each of the groups of claims identified above do not stand or fall together with any other claims or groups of claims for the reasons discussed in the Argument section below. In addition, each of claims 18, 19, 22, 24, and 25 do not stand or fall with any of the other claims for the reasons discussed in the Argument section.

VIII. ARGUMENT

A. The rejection of claims 1 and 2 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, and Wong should be REVERSED.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Wong. Claims 3 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Wong, and further in view of Simpson. The arguments below use claim 1 as representative of the group of claims including claims 1, 2, 3, and 6.

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543

(Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, Appellants' claim 1 recites a system comprising a master control processor and a bus controller connected to the master control processor. The bus controller implements a serial bus interface between the master control processor and a plurality of serial bus devices, the master control processor and the bus controller are on a first circuit board. A midplane is connected to the bus controller on the first circuit board. A plurality of additional circuit boards are connected to the serial bus interface through the midplane, each of the plurality of additional circuit boards includes one or more of the serial bus devices, a switch, and local control logic. The switch is configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state. The local control logic outputs a signal for controlling the state of the switch, the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state. Jobs, Atkinson, and Wong do not disclose or suggest this combination of features.

Jobs is directed to a system that includes a primary serial bus and one or more serial sub-buses separated from the primary serial bus by gating devices. (Jobs, Abstract). As disclosed in Fig. 2 of Jobs, gates, such as gates 206 and 208, are used to enable a selected one of sub-buses 214 and 216. (See Jobs, Fig. 2 and column 2, lines 26-46). This concept of creating sub-buses from a single bus, as disclosed by Jobs, is similar to the admitted conventional technique disclosed by Applicants in Fig. 1B. As shown in Fig. 1B of the pending application, a multiplexer 112 enables one of sub-buses 113 and 114 to be an active bus and isolates the non-active bus. (Specification, page 2, line 20 through page 3, line 5). As is further discussed in the specification, the bus system shown in Fig. 1B is not without its disadvantages. (Specification, page 3 line 6 through line 13).

In rejecting claim 1, the Examiner concedes that Jobs does not disclose many of the features recited in claim 1. Specifically, the Examiner states:

> Jobs does not teach the processor and bus controller being on a first circuit board; a midplane connected to the bus controller on the first circuit board; a plurality of additional circuit boards connected to the serial bus interface through the midplane; each additional board including one or more of the serial bus devices; local control logic for outputting a signal for controlling the state of the switch; and the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state.

(final Office Action, pages 2-3). The Examiner, however, contends that Atkinson discloses a midplane that includes a serial message bus connecting cards across the midplane and Wong discloses intelligent components, which are allegedly analogous to the switches recited in claim 1, that are connected to a bus which is

further connected to a master control unit. (final Office Action, page 3). According to the Examiner, one of ordinary skill in the art would have found it obvious to combine these teachings to obtain the invention recited in claim 1. (final Office Action, page 3). Appellants respectfully disagree.

Atkinson discloses a multiple application switching platform including a shelf that contains a midplane. (Atkinson, Abstract). Atkinson generally discloses that the midplane includes "message buses" 9A and 9B. (See Atkinson, col. 11, line 52 through col. 11, line 66). Although Atkinson may generally disclose busses between circuit boards that cross a midplane, nothing in Atkinson discloses or suggests that the circuit boards of Atkinson include the features recited in claim 1. Specifically, as recited in claim 1, each additional circuit board includes, for example, "a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state," and "local control logic for outputting a signal for controlling the state of the switch, the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state."

In stark contrast to the features recited in claim 1, the circuit cards of Atkinson, instead of including a switch to electrically isolate a non-selected circuit card from the bus, share the bus by pre-assigning a time slots to the circuit cards

(Atkinson, Abstract). Sharing a bus via time-slot sharing is significantly different than sharing a bus by controlling a switch state in response to a control signal from local control logic, as recited in claim 1. Further, the bus recited in claim 1 is a serial bus between a "master control processor and a plurality of serial bus devices." The busses of Atkinson pointed to by the Examiner ("Figure 1 Number 9", see final Office Action, page 3), however, are message busses that are used "for high speed peer to peer communications." (Atkinson, col. 11, lines 52-53). In this respect also, the disclosure of Atkinson is significantly different than the invention recited in claim 1.

The Examiner appears to additionally rely on Wong to disclose the switch and control logic recited in claim 1. Wong is directed to a fault-resilient automobile control system. The system of Wong includes a master control unit and a secondary control unit. (Wong, Abstract). The secondary control unit of Wong is a standalone computer that supports clients and other devices on a secondary support bus. (Wong, Abstract).

The Examiner particularly points to column 3, line 58 through column 4, line 7 of Wong for the disclosure of intelligent components. This section of Wong discloses:

> The master control unit 24 and the secondary control unit 26 are interconnected through the primary vehicle bus 28. In addition, various electronic automobile components are connected to the master control unit 24 via the primary bus 28. In this illustration, the electronic components include an antilock braking system (ABS) 32, an electronic steering system 34, and an engine control system 36. However, other components may likewise be connected to the primary vehicle bus 28, such as a security/alarm system, a diagnostic system, a lighting control system, a fuel injection system,

> an automatic transmission system, and so forth. In addition, the electronic components shown in FIG. 1 are intelligent components in that they each have their own local controller, typically embodied as a microprocessor. The automobile might further include non-intelligent electronic components which do not have local processing capabilities, as is explained below with reference to FIGS. 6-8.

Although this section of Wong mentions intelligent components, Appellants submit that this section of Wong fails to disclose or suggest the switch and the local control logic recited in claim 1. Although Wong generally mentions "switching logic," the switching logic of Wong is used to route data around a failed controller. (Wong, Abstract and col. 2, lines 51-56). Thus, the switching logic of Wong is in no way related to the switch recited in claim 1 on each of the additional circuit boards.

For at least these reasons, Appellants submit that Jobs, Atkinson, and Wong, alone or in combination, fail to disclose many of the features recited in claim 1. More specifically, none of these references disclose or suggest the particular combination of features included in the additional circuit boards recited in claim 1. Thus, Appellants submit that even if Jobs, Atkinson, and Wong were combined, the resulting combination would still not disclose or suggest each of the features recited in claim 1.

Appellants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) is additionally improper as there is no motivation to combine the references as the Examiner suggests. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly

or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See MPEP 2143.01. In the Office Action, the Examiner states that one of ordinary skill in the art would combine the references "to construct an open architecture that readily accommodates the insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson) ... and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong)." (final Office Action, pages 3-4). Appellants submit that these reasons given by the Examiner do not provide proper motivation to combine the references as the Examiner suggests.

For example, although constructing an open telephone switching architecture is listed as a benefit in the disclosure of Atkinson, Appellants submit that this motivation does not provide any reason to combine Atkinson with Jobs and Wong, as the Examiner suggests. Jobs and Wong are completely unrelated to open telephone switching architectures. Similarly, although Wong discloses a master control unit that provides backup for intelligent electronics components, Appellants submit that this motivation does not provide any reason to combine Wong with Jobs and Atkinson, as the Examiner suggests. The Examiner is merely listing stated features/advantages of the systems described by Wong and Atkinson. Virtually all patents include at least some general statement of the features or advantages of the patent. None of the features mentioned by the Examiner, however, suggest that Jobs, Atkinson, and Wong be combined to

obtain a system as the Examiner suggests and the alleged motivation does not satisfy the requirements of 35 U.S.C. § 103(a).

Accordingly, Appellants submit that the Examiner has not made a *prima facie* case of obviousness regarding claims 1 and 2. Accordingly, for these reasons also, the rejection of claim 1 should be reversed.

B. The rejection of dependent claims 3 and 6 under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Wong, as applied to claim 2, and further in view of Simpson, should be REVERSED.

The arguments below use claim 3 as representative of the group of claims including claims 3 and 6.

Claim 3 further defines the features of claim 2, and recites that the first circuit board further includes a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only one of the sub-buses being connected to the bus controller by the multiplexer at any given time. The Examiner relies on Simpson to disclose the features of claims 3 and 6.

Appellants submit that the Examiner has not made a *prima facie* case of obviousness with regard to claim 3. In applying Simpson, the Examiner states that it "would have been obvious to one of ordinary skill in the art ... in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson.)" (final Office Action, page 5). Appellants submit that the Examiner is simply restating the claimed features of Simpson. Nothing in

Simpson discloses or suggests that it would have been obvious to combine Simpson with Jobs, Atkinson, and Wong as the Examiner suggests. If anything, because Jobs discloses sub-buses that may support a maximum number of addressable devices (Jobs, Abstract), one of ordinary skill in the art would not be motivated to incorporate features of Simpson, because an expanded address space is already disclosed by Simpson.

C. The rejection of claims 4 and 5 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, Wong, Simpson, and further in view of Li and Baxter should be REVERSED.

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, Wong, and Simpson, and further in view of Li and Baxter. The arguments below use claim 4 as representative of the group of claims including claims 4 and 5.

Li is directed to a system and method to support out-band storage subsystem management via SCSI bus when operating power to a computer system is off. (Li, Title). The Examiner relies on Li for the disclosure of a temperature sensor and a voltage sensor. (final Office Action, page 6).

Baxter is directed to a high availability computer system. (Baxter, Title). The Examiner relies on Baxter for the disclosure of a ID EPROM device. (final Office Action, page 6).

Appellants submit that the Examiner has not made a *prima facie* case of obviousness regarding claims 4 and 5. In particular, Appellants submit that one

having ordinary skill in the art would not have been motivated to combine the six references applied by the Examiner. The Examiner states as motivation for incorporating Li and Baxter that it "would have been obvious ... in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter)." (final Office Action, pages 6 and 7). Appellants submit that this statement does not provide any reason to combine Li and Baxter with Jobs, Atkinson, Wong, and Simpson. The Examiner is merely listing stated features of the systems described by Li and Baxter. Such motivation does not satisfy the requirements of 35 U.S.C. § 103(a).

For at least these reasons, the Examiner has not provided proper motivation in rejecting claims 4 and 5, and the rejection of these claims should therefore be reversed.

D. The rejection of claims 7 and 8 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, Wong, and further in view of Posner should be REVERSED.

Dependent claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Wong, and further in view of Posner. The arguments below use claim 7 as representative of the group of claims including claims 7 and 8.

Claim 7, in contrast to Posner, further defines the additional circuit boards recited in claim 1 as including first, second, and third switches. The first switch selectively connects or disconnects a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus. The second switch selectively connects or disconnects the second portion of the serial bus to a third portion of the serial bus. The third switch selectively connects or disconnects the third portion of the serial bus to a fourth portion of the serial bus. The Examiner contends that these features of claim 7 are disclosed by Posner. (final Office Action, page 8). Appellants respectfully disagree.

Posner discloses a cross-connect switch. (Posner, Title). As defined by Posner, a cross-connect switch is a switching network which allows pairs of signal lines to be connected without disturbing connections between other lines connected by the cross-connect switch. (Posner, column 1, lines 9-12).

In contrast to Posner, claim 7 includes first, second, and third switches that selectively select or disconnect first, second, third, and fourth portions of a serial bus to one another. The switches of Posner, in contrast, are instead used to form a complete link between an input line and an output line. Thus, the features recited in claim 7 are significantly different than the cross-connect switches disclosed by Posner. The switches in Posner do not selectively select or disconnect portions of a serial bus. Posner merely creates or does not create a link. Accordingly, for at least this reason, Appellants submit that claim 7 is not disclosed or suggested by the combination of Jobs, Atkinson, Wong, and Posner.

Moreover, Appellants submit that there is no proper motivation to combine Posner with Jobs, Atkinson, and Wong. In attempting to provide motivation, the Examiner states that it "would have been obvious ... in order to allow the second portion of the bus to be connected to different first portions of the bus, the third portion of the bus to be connected to different second portions of the bus, and the fourth portion of the bus to be connected to different third portions of the bus (See Column 1 Lines 14-17 and Column 14 Lines 45-53 of Posner)." (final Office Action, page 8). The portions of Posner pointed to by the Examiner in columns 1 and 14 generally disclose that the cross-connect switch of Posner is constructed from a plurality of switching modules. Nowhere, however, does Posner disclose or suggest the specific connections between the first, second, and third switches, as recited in claim 7. If anything, the Examiner's statement of motivation appears to be a paraphrasing of Appellants' claim 7. Appellants submit that the Examiner is attempting to combine references with the benefit of information taken entirely from Appellants' specification.

In addressing Appellants' previous arguments regarding claim 7, the Examiner stated that the switch of Posner, "in addition to forming a complete link between an input and an output, also selectively connects and disconnects segments of the link." (final Office Action, page 25). Appellants submit that connecting segments to create a link is not the same as connecting portions of a serial bus. One example of the switches recited in claim 7 is shown in Appellants' Fig. 5. As shown, switches 430, 434, and 436 can be used to selectively connect different portions of the serial bus. Posner does not

selectively connect or disconnect different portions of a serial bus, as recited in claim 7, but instead selects various portions of a link to create one connected longer link. Each independent link portion selected by Posner cannot operate as a serial bus. Rather, the link portions must be selected together and in series to create a complete link.

For at least these reasons, Appellants submit that the rejection of claim 7 is improper and should be reversed.

E. The rejection of claims 9, 10, and 13 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, and Aggarwal should be REVERSED.

Claims 9, 10, and 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Aggarwal. The arguments below use claim 9 as representative of the group of claims including claims 9, 10, and 13.

Claim 9 is directed to a network device including a routing engine and a packet forwarding engine. The packet forwarding engine includes a midplane, a first circuit board having a master control processor, and a plurality of second circuit boards each having a control processor. The first and second circuit boards are electrically coupled through the midplane via a serial control bus. The second circuit boards each additionally include a switch configured to electrically connect the second circuit board to the first circuit board via the serial control bus when the switch is controlled to be in a first state and to electrically isolate the second circuit board from the serial control bus when the switch is controlled to

be in a second state. The switch of a particular one of the second circuit boards is in the first state only when the switches on each of the other of the second circuit boards are in the second state.

The Examiner contends that Jobs discloses a number of the features recited in claim 9, but concedes that Jobs does not disclose a routing engine, a packet forwarding engine including a midplane, and a plurality of second circuit boards each having a control processor. (final Office Action, page 10). Appellants initially note that if the routing engine, the packet forwarding engine including a midplane, and the plurality of second circuit boards that are currently recited in claim 9 were removed from this claim, the only remaining feature of claim 9 would be "a first circuit board having a master control processor."

The Examiner relies on Aggarwal as disclosing a routing engine and is apparently relying on Atkinson to disclose the remaining features of claim 9. (final Office Action, page 10). Aggarwal is directed to methods and systems for substituting use of the normal checksum field space in IP datagram headers for obviating current processing time and addressing space limitations. (Aggarwal, Abstract). Atkinson, as mentioned above, discloses a multiple application switching platform including a shelf that contains a midplane. (Atkinson, Abstract). Atkinson generally discloses that the midplane includes "message buses" 9A and 9B. (See Atkinson, col. 11, line 52 through col. 11, line 66).

Appellants submit that Jobs, Atkinson, and Aggarwal, even if combined as the Examiner suggests, still do not disclose or suggest each of the features recited in claim 9. For example, none of these references discloses or suggests

the plurality of second circuit boards recited in claim 9, where each includes a switch configured to electrically connect the second circuit board to the first circuit board via the serial control bus when the switch is controlled to be in a first state and to electrically isolate the second circuit board from the serial control bus when the switch is controlled to be in a second state, the switch of a particular one of the second circuit boards being in the first state only when the switches on each of the other of the second circuit boards are in the second state. Although Jobs may disclose a number of switches, the switches in Jobs are not included on a plurality of circuit boards and are not connected as recited in claim 9.

Additionally, Appellants submit that the rejection of claim 9 based on Jobs, Atkinson, and Aggarwal under 35 U.S.C. § 103(a) is additionally improper as there is no motivation to combine the references as the Examiner suggests. The Examiner picks and chooses various elements from the cited patents to obtain Appellants' invention. Appellants submit that such motivation does not satisfy the requirements of 35 U.S.C. § 103(a), as it relies entirely on hindsight gleaned only from Appellants' specification.

On pages 10 and 11 of the final Office Action, the Examiner lists a number of reasons why the Examiner believes it would be obvious to combine Jobs, Atkinson, and Aggarwal in the manner the Examiner suggests. Appellants have reviewed these reasons, and submit that each of the reasons corresponds to a feature or benefit discussed by one of Jobs, Atkinson, or Aggarwal. Although these reasons do relate to why one may wish to individually implement the

inventions of Jobs, Atkinson, and Aggarwal, none of these features suggest why one of ordinary skill in the art would be motivated to combine the various components of Jobs, Atkinson, and Aggarwal to obtain the invention recited in claim 9, which is significantly different than the disclosure of any of Jobs, Atkinson, and Aggarwal. Accordingly, Appellants submit that the Examiner has not presented a proper *prima facie* case of obviousness under 35 U.S.C. § 103(a), and the rejection of claims 9, 10, and 13 should therefore be reversed.

F. The rejection of claims 11 and 12 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, Aggarwal, and further in view of Wong should be REVERSED.

Dependent claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Aggarwal, and further in view of Wong. The arguments below use claim 11 as representative of the group of claims including claims 11 and 12.

Dependent claim 11 further defines the device of claim 9, and recites that the second circuit boards each additionally include local control logic connected to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic, the local control logic controlling the switch to be in the first or second state based on the received control information. Wong does not disclose or suggest these features of the claimed invention.

As previously mentioned, Wong is directed to a fault-resilient automobile control system. The system of Wong includes a master control unit and a

secondary control unit. (Wong, Abstract). The secondary control unit of Wong is a standalone computer that supports clients and other devices on a secondary support bus. (Wong, Abstract). The Examiner particularly points to column 3, line 58 through column 4, line 7 of Wong for the disclosure of intelligent components. This section of Wong has been reproduced above. Although this section of Wong mentions intelligent components, Appellants submit that this section of Wong completely fails to disclose or suggest the control logic recited in claim 11.

In addressing Appellants' previous arguments regarding claim 11, the Examiner states that "Wong teaches that a plurality of components, such as the switch of Jobs, can be connected to the primary bus, and that each component has a local controller (See Column 4 Lines 1-4)." (final Office Action, page 27). Appellants submit that Wong's disclosure of an intelligent component connected to a primary bus in no way discloses or suggest the features of claim 11, which include local control logic connected to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic, the local control logic controlling the switch to be in the first or second state based on the received control information.

Additionally, Appellants submit that the Examiner has not made a *prima facie* case of obviousness regarding Jobs, Atkinson, Aggarwal, and Wong. The Examiner states that it would have been obvious to combine Wong with Jobs, Atkinson, and Aggarwal "to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control

the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong)." (final Office Action, pages 13-14). Appellants submit that these reasons given by the Examiner do not provide proper motivation to combine the references as the Examiner suggests. The Examiner is merely listing stated features/advantages of the system described by Wong. Such motivation does not satisfy the requirements of 35 U.S.C. § 103(a).

Accordingly, for these reasons, in addition to their dependency, directly or indirectly, from claim 9, the rejection of claims 11 and 12 based on Jobs, Atkinson, Aggarwal, and Wong should be reversed.

G. The rejection of claims 14 and 17 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, Aggarwal and Simpson should be REVERSED. The rejection of claims 15 and 16 under 35 U.S.C. § 103(a) as unpatentable over Jobs, Atkinson, Aggarwal, Simpson, Li, and Baxter should be REVERSED.

Claims 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, and Aggarwal, as applied to claim 13, and further in view of Simpson. Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Jobs, Atkinson, Aggarwal, and Simpson, as applied to claim 14, and further in view of Li and Baxter. The arguments below use claim 14 as representative of the group of claims including claims 14-17.

Dependent claim 14 recites that the first circuit board further includes a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only

one of the sub-buses being connected to the bus controller by the multiplexer at any given time. The Examiner contends that Simpson discloses the features of claim 14, and that one of ordinary skill in the art would have found it obvious to modify Jobs, Atkinson, and Aggarwal, in view of Simpson, to obtain the invention recited in claim 14.

Appellants submit that the Examiner has not made a *prima facie* case of obviousness with regard to claim 14. In applying Simpson, the Examiner states that it "would have been obvious to one of ordinary skill in the art ... in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson.)" (final Office Action, page 15). Again, Appellants submit that the Examiner is simply restating the claimed features of Simpson. Nothing in Simpson discloses or suggests that it would have been obvious to combine Simpson with Jobs, Atkinson, and Aggarwal as the Examiner suggests. If anything, because Jobs discloses sub-buses that may support a maximum number of addressable devices (Jobs, Abstract), one of ordinary skill in the art would not be motivated to incorporate features of Simpson, because an expanded address space is already disclosed by Simpson.

For at least these reasons, the rejections of claim 14 and 17 should be reversed.

H. The rejection of claim 18 under 35 U.S.C. § 103(a) as unpatentable over Atkinson, Posner, and Wong should be REVERSED.

The Examiner appears rely on Atkinson for the disclosure of the local processor and the bus controller recited in claim 18. (final Office Action, page 17). Additionally, the Examiner relies on Posner to disclose the first, second, and third switches recited in claim 18. (final Office Action, pages 17 and 18). Finally, the Examiner relies on Wong. (final Office Action, page 18).

In contrast to Atkinson, Posner, or Wong, claim 18 is directed to a circuit board that includes, among other things, a first switch for selectively connecting or disconnecting a first portion of a two wire serial bus from an external circuit board to a second portion of the two wire serial bus; a second switch for selectively connecting or disconnecting the second portion of the two wire serial bus to a third portion of the two wire serial bus; and a third switch for selectively connecting or disconnecting the third portion of the two wire serial bus to a fourth portion of the two wire serial bus. Appellants submit that the cited references completely fail to disclose or suggest these features of claim 18.

Posner, in particular, discloses a cross-connect switch. A cross-connect switch does not disclose or suggest the switches recited in claim 18, which selectively connect or disconnect first, second, third, and fourth portions of a two wire serial bus to one another. The cross-connect switches of Posner are instead used to form a complete link between an input line and an output line. Thus, the features recited in claim 18 are significantly different than the cross-connect switches disclosed by Posner.

As the Examiner conceded in the final Office Action, Atkinson also does not disclose the first, second, or third switches recited in claim 18. (final Office Action, page 17).

Wong also does not disclose or suggest the first, second, or third switches recited in claim 18. The Examiner appears to contend that the "intelligent components" disclosed by Wong are equivalent to the first, second, and third switches recited in claim 18. (final Office Action, page 18). Appellants strongly disagree. The intelligent components of Wong are described as the electronic components shown in Fig. 1, (Wong, col. 4, lines 1-3), which include, for example, an antilock braking system 32, an electronic steering system 34, and an engine control system 36. These "intelligent components" of Wong in no way disclose or suggest a first switch for selectively connecting or disconnecting a first portion of a two wire serial bus from an external circuit board to a second portion of the two wire serial bus; a second switch for selectively connecting or disconnecting the second portion of the two wire serial bus to a third portion of the two wire serial bus; and a third switch for selectively connecting or disconnecting the third portion of the two wire serial bus to a fourth portion of the two wire serial bus, as recited in claim 18.

In addressing Appellants' previous arguments regarding claim 18, the Examiner stated that the switch of Posner, "in addition to forming a complete link between an input and an output, also selectively connects and disconnects segments of the link." (final Office Actions, page 27). Appellants submit that connecting segments to create a link is not the same as connecting portions of a

serial bus. Posner does not selectively connect or disconnect different portions of a serial bus, as recited in claim 18, but instead selects various portions of a link to create one connected longer link. Each independent link portion selected by Posner cannot operate as a serial bus. Rather, the link portions must be selected together and in series to create a complete link.

Because Atkinson, Posner, and Wong, taken in combination, do not disclose or suggest each of the features of claim 18, Appellants submit that the rejection of claim 18 is improper and should be reversed. The Examiner is simply picking and choosing various elements from the cited patents to obtain Applicants' invention. Appellants submit that this is not a proper rejection under 35 U.S.C. § 103(a), as it relies entirely on hindsight gleaned only from Appellants' specification.

I. The rejection of dependent claim 19 under 35 U.S.C. § 103(a) as unpatentable over Atkinson, Posner, and Wong should be REVERSED.

Claim 19 further defines the features of claim 18, and recites that the local control logic circuit operates to connect the external circuit board and the local processor to different portions of the two wire serial bus. The Examiner appears to contend that the features of claim 19 are disclosed by Posner. Posner, however, never mentions a two wire serial bus, much less connecting an external circuit board and a local processor to different portions of a two wire serial bus.

The Examiner points to column 14, lines 38-40 of Posner as disclosing the features recited in claim 19. (final Office Action, page 19). This section of Posner merely states that "[c]ross-connect switch 360 may then be viewed as a three stage switch having a center stage constructed from two switch modules having 9 input lines and 18 output lines." Appellants submit that a three-stage cross-connect switch is merely a cross-connect switch that is designed to connect a particular input line to a particular output line along a three-stage path. This is not equivalent to the features recited in claim 19.

Accordingly, Appellants submit that Posner does not disclose or suggest the features of claim 19. Accordingly, the rejection of claim 19 is improper and should be reversed.

J. The rejection of claim 22 under 35 U.S.C. § 103(a) as unpatentable over Atkinson, Posner, and Wong, and further in view of Loftis, should be REVERSED.

Claim 22 further defines the features of claim 18, and recites that the local control logic circuit controls the first, second, and third switches so that if the first switch is disconnected, the second and third switch are controlled by the local processor. The Examiner points to the Abstract, Figs. 1 and 2, and column 2, lines 14-21 of Loftis as allegedly disclosing this feature of the invention. Column 2, lines 14-21 of Loftis state:

> The signal, preferably a pulse having a predetermined pulsewidth, is tested for validity by the electronic switch and, if valid, triggers the electronic switch to electrically isolate the faulty computer from the process control I/O data acquisition/control units and to

> electrically couple the back-up computer to the process control I/O data acquisition/control units.

This section of Loftis relates to isolating a faulty computer and enabling a back-up computer. Appellants submit that this section of Loftis in no way discloses or suggests local control logic controlling first, second, and third switches as recited in claim 22. Appellants additionally note that claim 22 does not simply claim any switches, but, as recited in claim 18, is directed to switches that selectively connect or disconnect portions of a two wire serial bus.

For at least these reasons, Appellants submit that Loftis does not cure the deficiencies of Atkinson, Posner, and Wong. Accordingly, the rejection of claim 22 under 35 U.S.C. § 103(a) is improper and should be reversed.

K. The rejection of claim 24 under 35 U.S.C. § 103(a) as unpatentable over Atkinson, Posner, and Wong, and further in view of Li should be REVERSED.

Claim 24 further defines the features of claim 18, and recites that wherein at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus. The Examiner relies on Li to disclose the features of claim 24. (final Office Action, page 21). Although Li may disclose a voltage monitor and a temperature sensor, Appellants submit that Li does not disclose or suggest that these devices are connected to a second portion of a two wire serial bus, as recited in claim 24. Further, nothing in Li or any of the other applied references suggests that a voltage monitor and a temperature sensor be connected the second portion of a two wire serial bus. Accordingly,

the rejection of claim 24 under 35 U.S.C. § 103(a) is improper and should be reversed.

L. The rejection of claim 25 under 35 U.S.C. § 103(a) as unpatentable over Atkinson, Posner, and Wong, and further in view of Baxter should be REVERSED.

Claim 25 further defines the features of claim 18, and recites that an ID EPROM is connected to the third portion of the two wire serial bus. The Examiner relies on Baxter to disclose the features of claim 25. (final Office Action, page 22). Although Baxter may disclose an EPROM, Appellants submit that Baxter does not disclose or suggest an ID EPROM connected to a third portion of a two wire serial bus, as recited in claim 25. Further, nothing in Baxter or any of the other applied references suggests that an ID EPROM be connected the third portion of the two wire serial bus recited in claim 25. Accordingly, the rejection under 35 U.S.C. § 103(a) is improper and should be reversed.

VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejection of claims 1-19, 22, 24, and 25 under 35 U.S.C. § 103(a).

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,
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Attachment: Appendix with Listing of Claims

APPENDIX

1. (original) A system comprising:

a master control processor;

a bus controller connected to the master control processor and implementing a serial bus interface between the master control processor and a plurality of serial bus devices, the master control processor and the bus controller being on a first circuit board;

a midplane connected to the bus controller on the first circuit board; and

a plurality of additional circuit boards connected to the serial bus interface through the midplane, each of the plurality of additional circuit boards including

one or more of the serial bus devices,

a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state, and

local control logic for outputting a signal for controlling the state of the switch, the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state.

2. (original) The system of claim 1, wherein the first circuit board further comprises:

a master control logic circuit connected to the master control processor, the master control logic circuit communicating with the local control logic of each of the additional circuit boards over the midplane.

3. (original) The system of claim 2, wherein the first circuit board further comprises:

a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only one of the sub-buses being connected to the bus controller by the multiplexer at any given time.

4. (original) The system of claim 3, wherein the serial bus devices include at least one of a temperature sensor, a voltage monitor, and an ID EPROM.

5. (original) The system of claim 3, wherein one of the serial bus devices includes an ID EPROM connected to the midplane.

6. (original) The system of claim 3, wherein one of the sub-buses is connected to the plurality of additional circuit boards .

7. (original) The system of claim 1, wherein each of the plurality of additional circuit boards includes:

a first switch for selectively connecting or disconnecting a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus;

a second switch for selectively connecting or disconnecting the second portion of the serial bus to a third portion of the serial bus; and

a third switch for selectively connecting or disconnecting the third portion of the serial bus to a fourth portion of the serial bus.

8. (original) The system of claim 7, wherein each of the plurality of additional circuit boards further includes:

a local processor; and

a bus controller interfacing the local processor to the fourth portion of the serial bus;

the local control logic circuit being connected to receive control information from the first circuit board and the local processor and control the first, second, and third switches based on the received control information.

9. (original) A network device in a computer network comprising:

a routing engine for consolidating routing information learned from routing protocols in the network; and

a packet forwarding engine connected to the routing engine, the packet forwarding engine including

a midplane;

a first circuit board having a master control processor; and

a plurality of second circuit boards each having a control processor, the first and second circuit boards being electrically coupled through the midplane via a serial control bus, the second circuit boards each additionally including a switch configured to electrically connect the second circuit board to the first circuit board via the serial control bus when the switch is controlled to be in a first state and to electrically isolate the second circuit board from the serial control bus when the switch is controlled to be in a second state, the switch of a particular one of the second circuit boards being in the first state only when the switches on each of the other of the second circuit boards are in the second state.

10. (original) The network device of claim 9, wherein the network device is a network router.

11. (original) The network device of claim 9, wherein the plurality of second circuit boards each additionally comprises:

local control logic connected to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic, the local control logic controlling the switch to be in the first or second state based on the received control information.

12. (original) The network device of claim 11, wherein the first circuit board further comprises:

a master control logic circuit connected to the master control processor, the master control logic circuit communicating with the local control logic of each of the second circuit boards over the midplane.

13. (original) The network device of claim 9, wherein the first circuit board further comprises:

a bus controller connected to the master control processor and implementing an interface for the serial bus.

14. (original) The network device of claim 13, wherein the first circuit board further comprises:

a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only one of the sub-buses being connected to the bus controller by the multiplexer at any given time.

15. (original) The network device of claim 14, wherein one of the sub-buses includes, as a bus device, at least one of a temperature sensor, a voltage monitor, and an ID EPROM.

16. (original) The network device of claim 14, wherein one of the sub-buses includes, as a bus device, an ID EPROM connected to the midplane.

17. (original) The network device of claim 14, wherein one of the sub-buses is connected to the plurality of second circuit boards.

18. (original) A circuit board comprising:

a first switch for selectively connecting or disconnecting a first portion of a two wire serial bus from an external circuit board to a second portion of the two wire serial bus;

a second switch for selectively connecting or disconnecting the second portion of the two wire serial bus to a third portion of the two wire serial bus;

a third switch for selectively connecting or disconnecting the third portion of the two wire serial bus to a fourth portion of the two wire serial bus;

a local processor;

a bus controller interfacing the local processor to the fourth portion of the two wire serial bus; and

a local control logic circuit connected to receive control information from the external circuit board and the local processor and control the first, second, and third switches based on the received control information.

19. (original) The circuit board of claim 18, wherein the local control logic circuit operates to connect the external circuit board and the local processor to different portions of the two wire serial bus.

20. (original) The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first and second switches are connected, the third switch is disconnected.

21. (original) The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first switch is connected and the second switch is disconnected, the third switch is connected.

22. (original) The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first switch is disconnected, the second and third switch are controlled by the local processor.

23. (cancelled)

24. (original) The circuit board of claim 18, wherein at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus.

25. (original) The circuit board of claim 18, wherein an ID EPROM is connected to the third portion of the two wire serial bus.